UNIT- IV

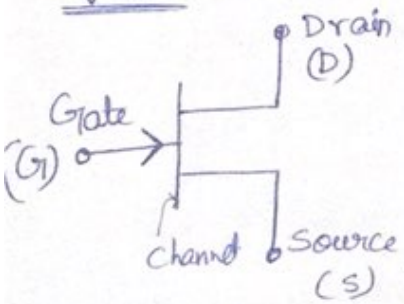
Junction Field Effect Transistor

FET : field effect transistor :- FET is a voltage controlled device, i.e., its output characteristics are controlled by applied input voltage.

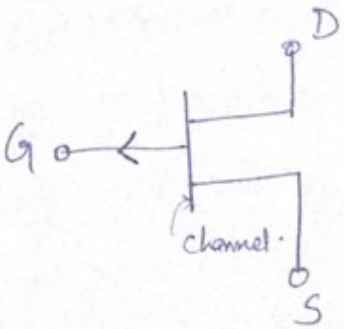
→ Current flow in FET is due to only one type of carrier, i.e., either holes (or) electrons, hence it is called a uni-polar device.

→
- FET
  - JFET
    - n-channel JFET
    - p-channel JFET
  - MOSFET
    - n-channel MOSFET
    - p-channel JFET

Symbols :



n-channel JFET



p-channel JFET

Construction of n-channel JFET :-

Step1: Initially n-type semiconductor bar is considered to construct n-channel JFET.

Step2: Heavily doped two p-type semiconductors are diffused on opposite sides of n-type semiconductor.

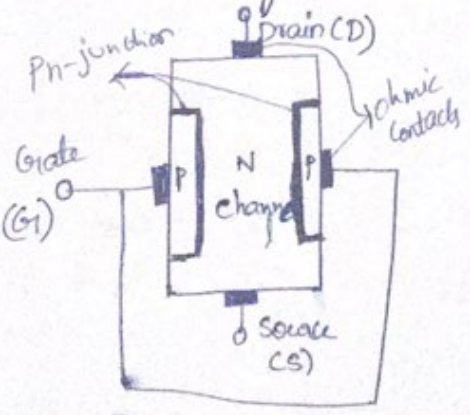
Step3: As a result two pn-junctions are formed. The region b/w these two pn-junctions is called as "channel".

Step4: As channel is in n-type semiconductor, the resultant is known as n-channel JFET.

Step5: Ohmic contacts are made at the ends of
a) n-type semiconductor &
b) P-type semiconductor.

Step6: Ohmic contacts made at n-type semiconductor are called as source & drain.

* Ohmic contacts of two P-type semiconductors are internally connected and resultant is called as gate.



Construction of P-channel JFET:

Step1: Initially p-type semiconductor bar is considered to construct p-channel JFET.

Step2: Heavily doped n^+ n-tye sc are diffused on opposite sides of p-type semiconductor

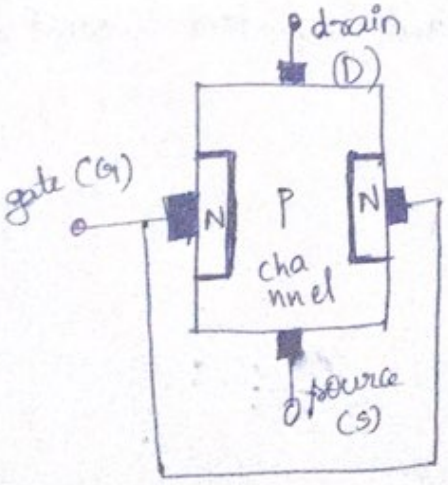
Step3: As a result two pn-junctions are formed. The region b/w these two pn-junctions is called "channel"

Step4: As channel is in p-type sc. the resultant is known as p-channel JFET.

Step5: Ohmic contacts are made at the ends of
① p-type sc ② n-type sc

Step6: Ohmic contacts made at p-type sc are known as source and drain.

* ohmic contacts of two n-type sc are internally connected and resultant is called as gate.

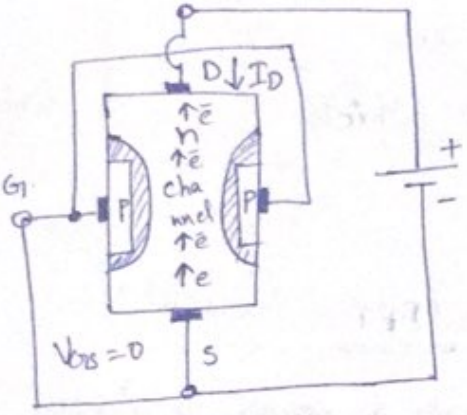


Principle of operation of n-channel JFET :

→ In JFET the pn-junction b/w gate & source is always kept in reverse biased conditions. V_{DS} is applied in such a way that majority carriers flow from source to drain.

Case(1) : $V_{GS} = 0$ with applied V_{DS}

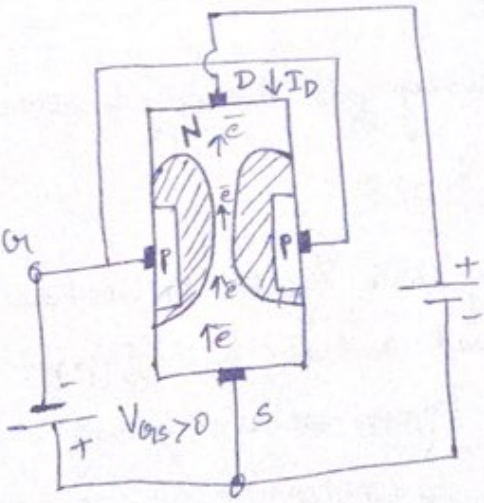
→ By connecting gate directly to source terminal, $V_{GS} = 0$



→ Initially with $V_{GS}=0$, pn junctions are formed and due to diffusion depletion layers are also formed around pn-junctions.

→ with applied V_{DS}, majority charge carriers i.e $\bar{e}$s start flowing from source to drain and produces drain current I_D in opposite direction to the flow of $\bar{e}$s. with $V_{GS}=0$ maximum I_D is produced.

Case (2) : $V_{GS} > 0$, with applied V_{DS}



→ When (-ve) voltage V_{GS} is increased then width of depletion regions increase and it will penetrate more toward the drain terminal.

→ As width of the depletion reg increase, width of the channel decreases.

→ If width of the channel decreases then the no of $\bar{e}$s

flowing from source to drain decreases and hence the drain current I_D decreases.

Cut-off voltage :- If we keep on increasing the reverse voltage V_{GS} then there will be a stage, at which width of the depletion region is equal to width of channel.

→ At this stage no es can move from source to drain as a result drain current is zero.

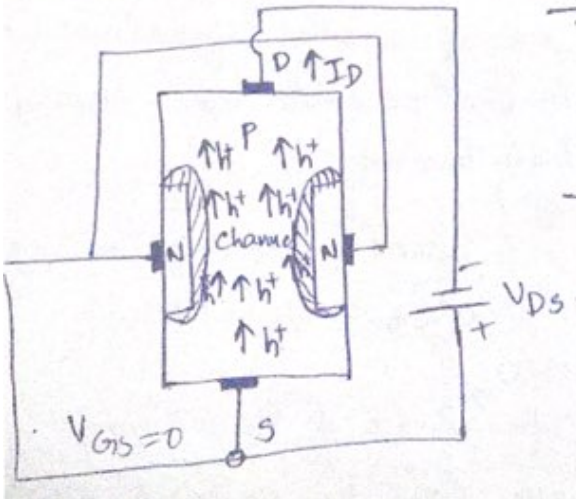
→ The reverse voltage V_{GS} at which $I_D = 0$ is said to be "cut-off voltage".

Principle of operation of P-channel JFET

→ In JFET the Pn-junction b/w gate & source is always kept in reverse biased condition.

→ V_{DS} is applied in such a way that majority carriers should flow from source to drain.

Case(1): $V_{GS} = 0$ with applied V_{DS}



→ By connecting gate directly to source terminal, $V_{GS} = 0$.

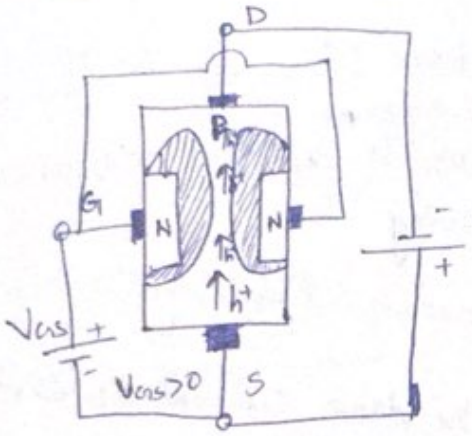
→ Initially with $V_{GS} = 0$, Pn junctions are formed and due to diffusion depletion layers are also formed around pn-junctions.

→ with applied V_{DS}, majority charge carriers i.e., holes start flowing from source to drain and produces drain current.

→ I_D is in the same direction to the flow of holes.

→ with $V_{GS} = 0$, maximum I_D is produced.

Case(2): $V_{GS} > 0$ with applied V_{DS}

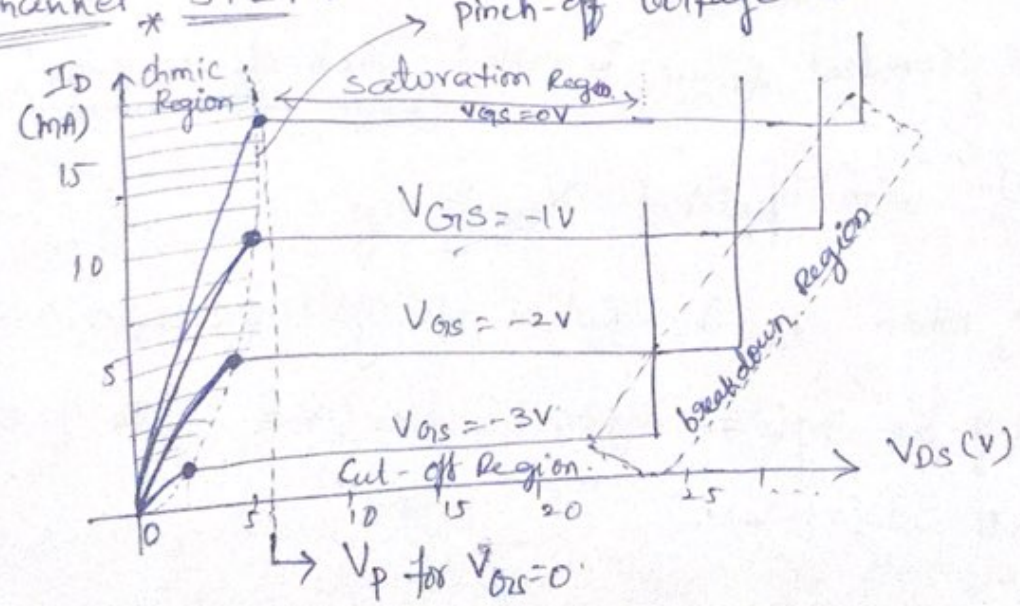


→ When (+ve) voltage V_{GS} is increased. then width of the depletion regions increases and it will penetrate more towards drain terminal.

→ As width of the depletion region increases, width of the channel decreases

→ If width of the channel decreases then the no: of holes flowing from source to drain decreases and hence the drain current I_D decreases

Drain characteristics (or) Volt-ampere Characteristics of n-channel JFET:



→ Graphical relation b/w drain current I_D and V_{DS} for various V_{GS} values represents "drain characteristics".

Case (1): with V_{GS} & V_{DS} at zero

→ where $V_{GS}=0$ & $V_{DS}=0$, no drain current flows. $I_D=0$

Case (2): self pinch off at no bias ($V_{GS}=0$), $V_{DS}>0$

→ When $V_{GS}=0$ and when a small amount of V_{DS} is applied, then I_D i.e drain current starts flowing.

→ with increase in V_{DS}, I_D increases linearly.

→ At some value of V_{DS}, the drain current I_D can't be increased further.

→ Any additional increase in V_{DS} has no effect on drain current I_D.

→ The voltage V_{DS} at which the current I_D reaches its constant value is called "pinch-off voltage" V_p.

Case (3): with applied V_{GS} & V_{DS}

→ When V_{GS} is applied b/w gate & source, then width of the depletion region increases and width of the channel decreases.

→ As a result drain current I_D decreases i.e Pinch-off voltage is reached at lower I_D than when $V_{GS} = 0$.

→ For more negative values of V_{GS}, the pinch off voltage is reached at lesser values of I_D.

Ohmic Region: The region in which drain current I_D increases linearly w.r.t V_{DS} is called as "ohmic Region"

Saturation Region: The region in which drain current I_D doesn't vary w.r.t V_{DS} (i.e., I_D is constant is called "saturation Region".

Breakdown Region: If we further increase V_{DS}, then voltage across the channel increases and cause the breakage of gate-channel junction due to avalanche effect.

→ At this point drain current increases rapidly, and device is said to be damaged.

→ The region in which I_D increases rapidly due to break-down of gate-channel is called as "breakdown region".

Cut-off Region: The region under the O/P curve at highest negative voltage V_{GS} is called "cut-off Region". When $V_{GS} = -V_p$ then $I_D = 0$

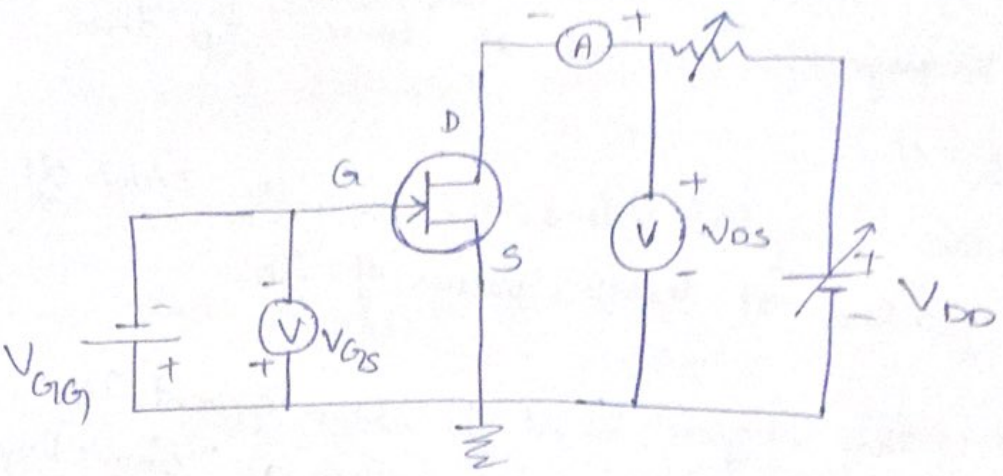
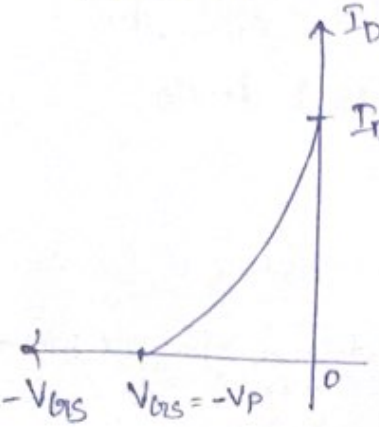


fig: experimental setup to plot n-channel JFET

Transfer characteristics of n-channel JFET

The graphical relation b/w drain current I_D and V_{GS} at constant V_{DS} represents the "transfer characteristics" of n-channel JFET.



→ From graph it can be observed that, I_D is max at $V_{GS} = 0$. And it is represented with I_{DSS}.

→ At $V_{GS} = -V_P$, $I_D = 0$.

→ I_D & V_{GS} has a non-linear relationship, this relationship is called as "Shockley's" eqn. i.e.,

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$$

$$\Rightarrow \left[1 - \frac{V_{GS}}{V_P}\right]^2 = \frac{I_D}{I_{DSS}}$$

$$1 - \frac{V_{GS}}{V_P} = \sqrt{\frac{I_D}{I_{DSS}}}$$

$$\frac{V_{GS}}{V_P} = 1 - \sqrt{\frac{I_D}{I_{DSS}}}$$

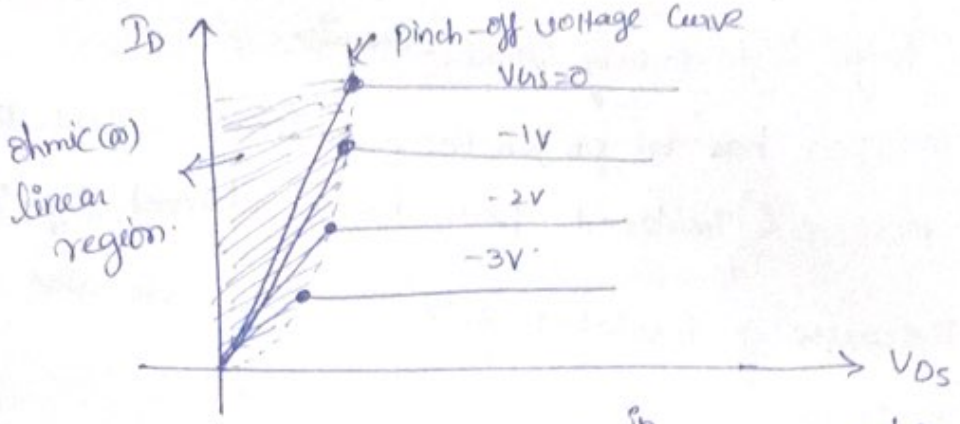
$$\boxed{V_{GS} = V_P\left[1 - \sqrt{\frac{I_D}{I_{DSS}}}\right]}$$

Comparison between JFET & BJT

JFET	BJT
→ It is a unipolar device	→ It is a bipolar device
→ It is a voltage controlled device	→ It is a current controlled device.
→ The i/p resistance is very high as V_{GS} is reverse biased	→ i/p resistance is low as Je junction is forward biased
→ It has a (-ve) temperature coefficient i.e., current decreases if temperature increases	→ It has (+ve) temperature coefficient i.e current increases if temperature increases.
→ FETs occupy less silicon space hence easier to fabricate ie small in size	→ BJT require more silicon space i.e large in size.
→ less noisy than BJT	→ Noisier than FET
→ FETs are costlier than BJTs	→ BJTs are cheaper

FET as a Voltage Variable Resistor

Let us consider drain characteristics of FET



→ It can be observed that in the region before Pinch-off voltage curve drain characteristics are linear. In this region drain to source resistance is controlled by V_{GS}.

→ Hence in this ohmic (or) linear region, FET is used as voltage-controlled resistor (or) voltage variable resistor (VVR) (or) voltage-dependent-resistor (VDR).

→ In JFET drain to source conductance is given by

$$g_d = \frac{I_D}{V_{DS}} \rightarrow (1)$$

for small value of V_{DS}, (1) can be written as

$$g_d = g_{do}\left[\sqrt{1-\frac{V_{GS}}{V_p}}\right]$$

g_{do} = drain conductance at $V_{GS}=0$.

→ drain resistance w.r.t V_{GS} is given by.

$$r_d = \frac{r_0}{1-KV_{GS}}$$

r_0 → drain resistance at $V_{GS}=0$

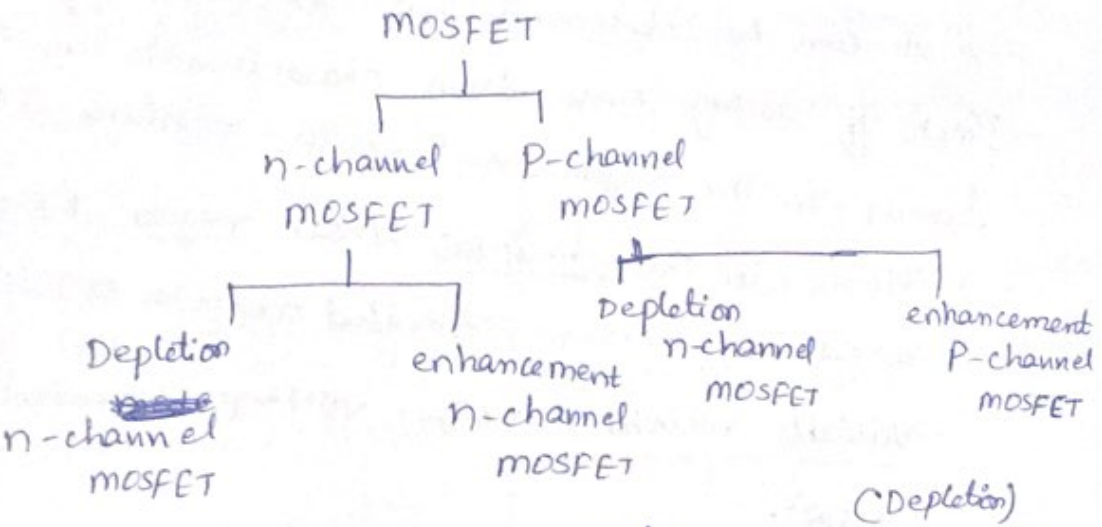
K → Constant

MOSFET :- Metal oxide Semiconductor field effect transistor.

→ MOSFETs are of small in size and hence can be used to design high density VLSI circuits.

→ MOSFET has no pn junction structure; instead, the gate of MOSFET is insulated from channel channel by SiO_2 layer.

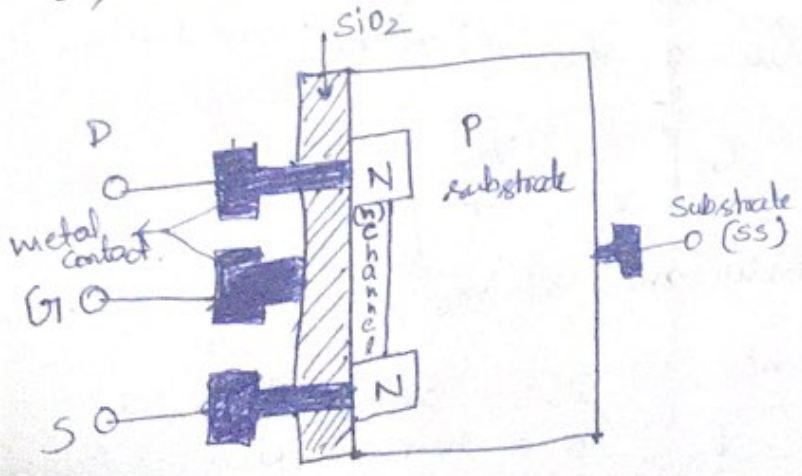
→ Because of insulated gate, MOSFETs are also called IGFETs.



Construction, operation, characteristics of (Depletion) D-MOSFET

Construction:

→ Let us consider n-channel DMOSFET.



→ To construct n-channel DMOSFET, initially p-type sc sub-shrate is considered.

→ Two highly doped n-type sc are diffused into P-sub-shrate.

→ In DMOSFET. channel is in-built b/w diffused n-type sc, and is called as n-channel.

→ Metal contacts are made w.r.t, N-type sc, P-type sc and SiO_2 layer.

→ source & drain terminals are extracted from N-type sc through metal contact

→ gate terminal is extracted from SiO_2 layer through metal contact

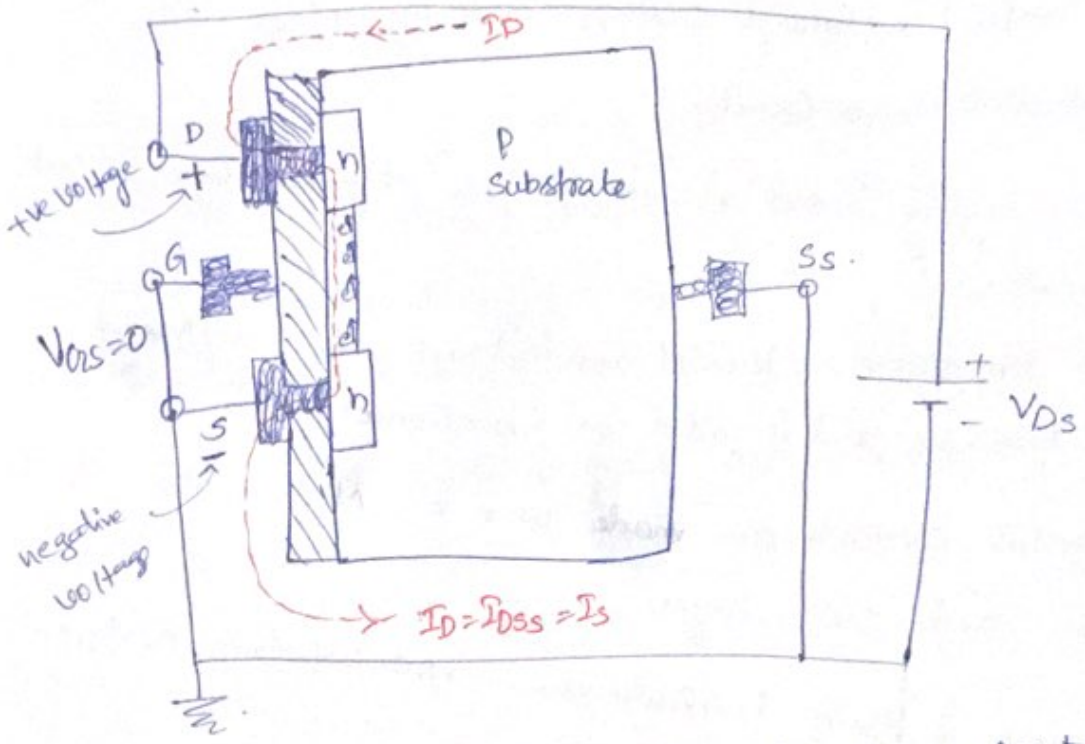
→ substrate is extracted from P-type sc through metal contact.

→ SiO_2 is an insulating layer.

→ source & drain terminals are in contact with channel via n-type sc but not gate terminal.

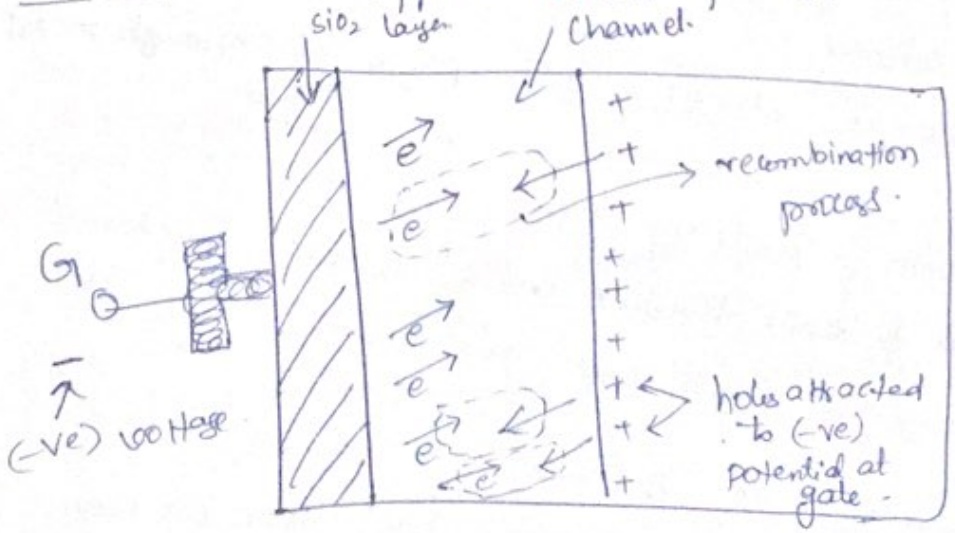
Operation: Case(1): $V_{GS} = 0$ with applied V_{DS}

→ When $V_{GS} = 0$ with applied V_{DS}, then $\bar{e}$s move from source to drain and result the drain current in opposite direction.



→ V_{GS} is maintained 'zero' by shorting G & S terminals

Case(i): with applied $-V_{GS}$ & V_{DS}.

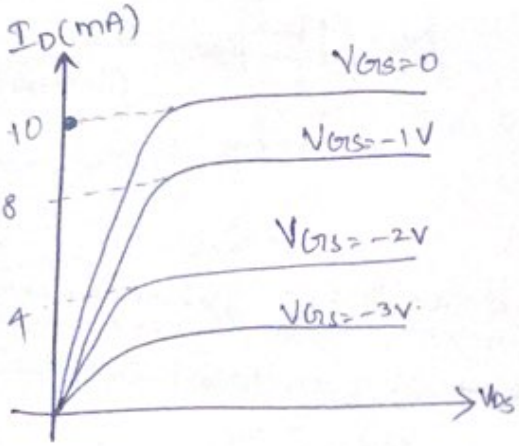


→ When gate terminal is provided with negative voltage, then this (-ve) voltage tend to pressure electrons towards p-type substrate.

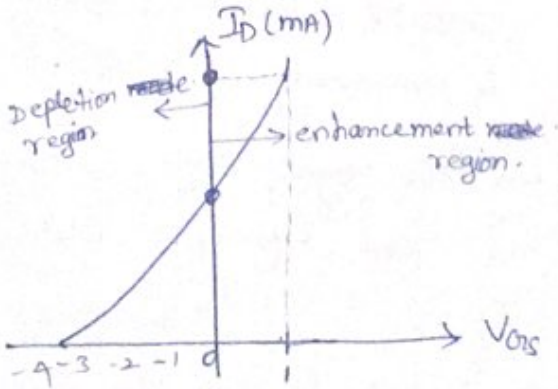
→ This (-ve) gate voltage initiates the recombination of ēs and holes

→ If this (-ve) gate voltage is increased, then the no: of recombinations of ēs & holes increases, as a result no: of free ēs in the channel decreases.

→ As the no: of free ēs in channel is decreased, drain current I_D will also decreases.



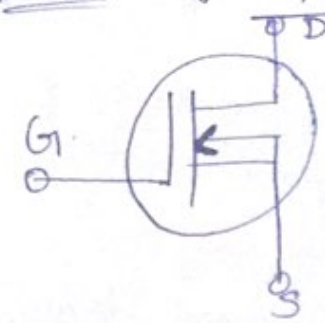
Case (3): with applied +V_{GS} & V_{DS}.



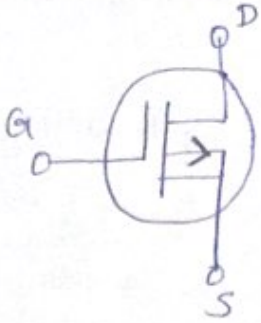
→ When gate terminal is provided with (+ve) voltage, then drain current I_D increases rapidly.

→ (+ve) voltage at gate terminal enhanced the I_D value than, the I_D at $V_{GS}=0$, the region on (+ve) V_{GS} of characteristics is said to be "enhancement region".

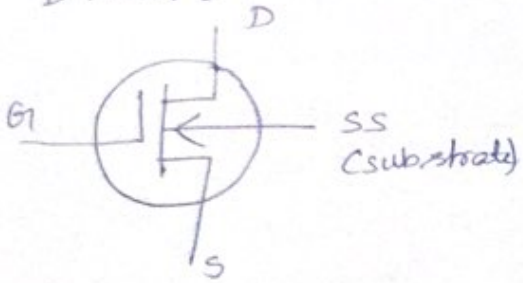
Symbols of depletion MOSFET

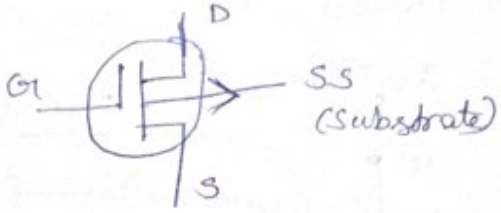


n-channel DMOSFET



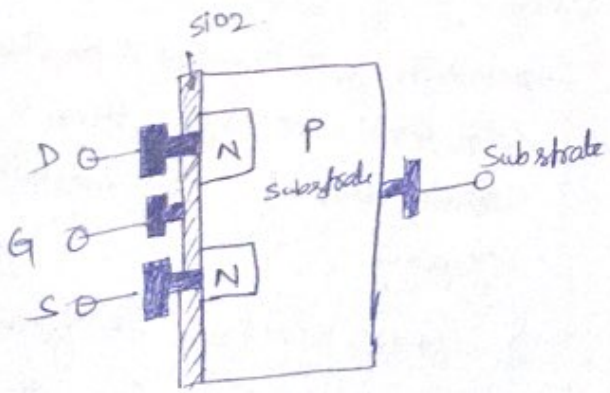
p-channel DMOSFET.





Construction, Operation, characteristics of Enhancement (or) EMOSFET:

Let us consider construction of n-channel EMOSFET



→ To construct n-channel EMOSFET, initiall p-type s.c is considered

→ Two highly doped n-type s.c are diffused into p-type sc

→ An SiO_2 layer is developed on one side of p-type s.c

→ 4 metal contacts are made w.r.t. n, p-type sc & SiO_2 layer.

→ Metal contact made w.r.t n-type SC are called as source & drain terminals

→ Metal contact made w.r.t p-type SC is known as substrate

→ metal contact made w.r.t SiO_2 is called as gate terminal

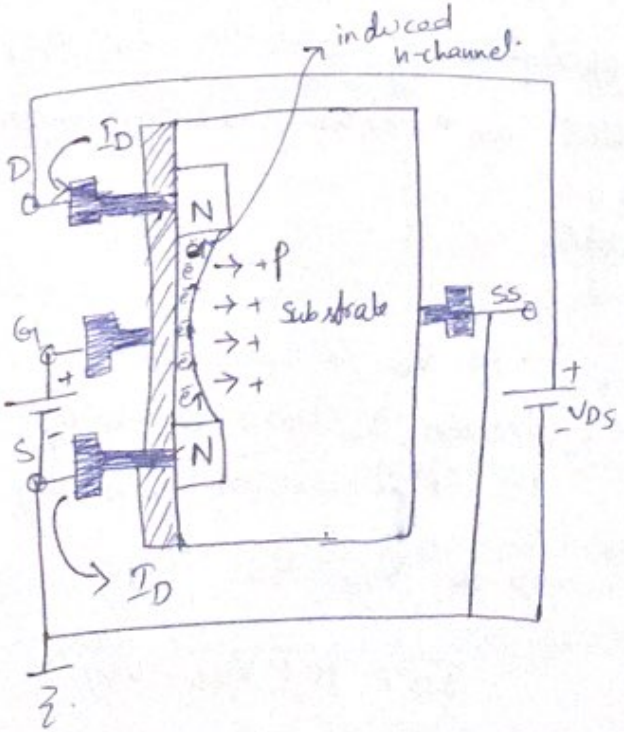
→ But the channel b/w two n-regions is absent in enhancement type MOSFET.

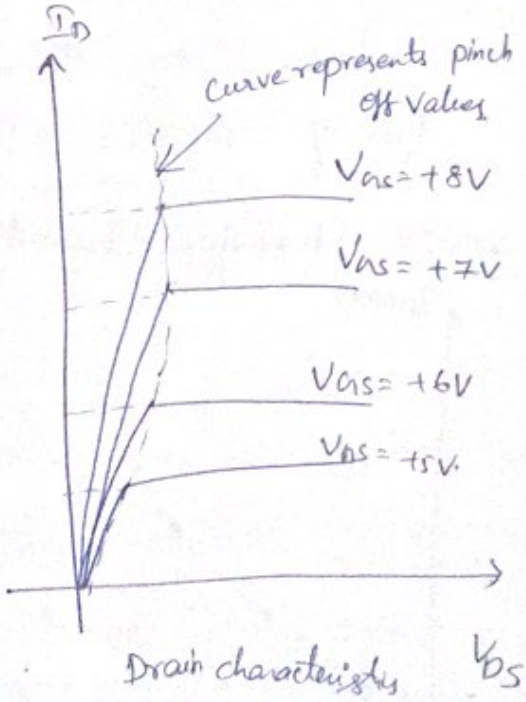
Operation & characteristics

Case(1): with $V_{GS}=0$ & with applied V_{DS}

→ Practically when V_{DS} is applied with $V_{GS}=0$, zero current flows

Case(2): with applied (+ve) V_{GS} & V_{DS}.





→ When V_{GS} is applied in (+ve) direction, the concentration of e^-s near SiO_2 surface increases.

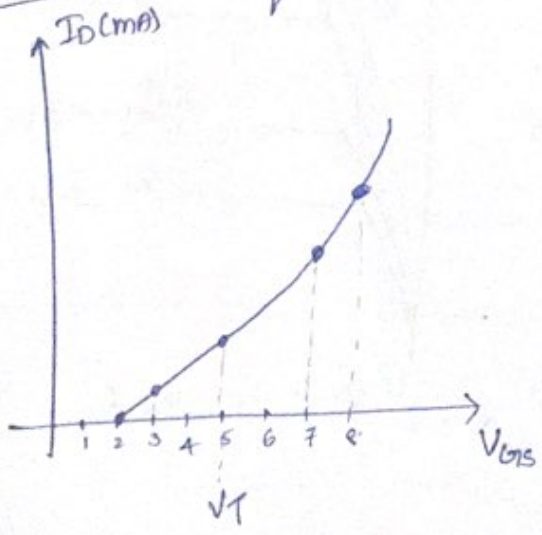
→ At a particular value of V_{GS}, there is a measurable current flow b/w drain & source. This value of V_{GS} is called "Threshold voltage (V_T)".

→ When (+ve) V_{GS} is increased greater than V_T, then it induces a channel. And hence drain current I_D flows

→ For any voltage below threshold voltage, there is no channel.

→ Since channel doesn't exist with $V_{GS}=0V$ and "enhanced" by the application of positive V_{GS}, this type of MOSFET is called an "enhancement type MOSFET"

Case(3): transfer characteristics



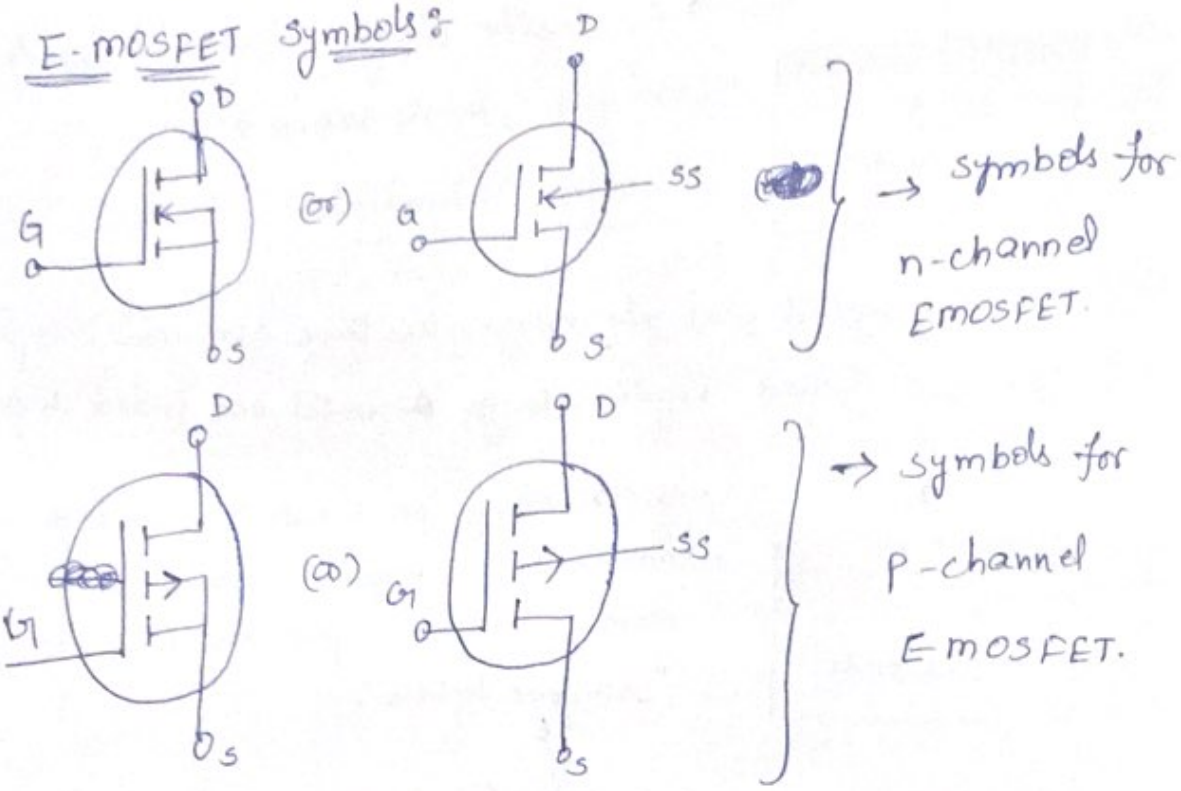
→ As V_{GS} increases in (+ve) direction, I_D increases rapidly i.e it increases non linearly

→ for $V_{GS} > V_T$.

$$I_D = K(V_{GS} - V_T)^2$$

where K ⇒ conduction parameter.

E-MOSFET symbols:



MOSFET As a Capacitor:

→ An MOS capacitor is made of a semiconductor body (or) substrate, an insulator and a metal electrode.

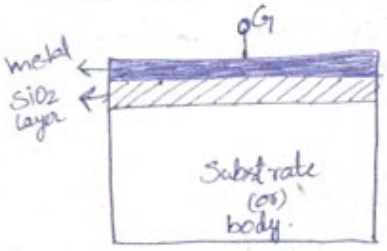


fig: MOSFET as capacitor structure

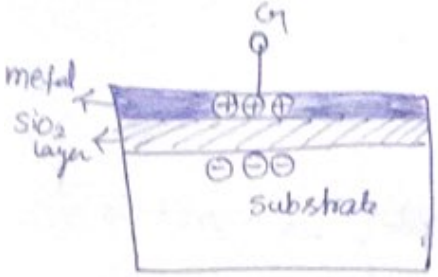
→ The metal acts as one plate of the capacitor, substrate (P-type (or) N-type sc) acts as another plate of capacitor, SiO_2 layer acts as an insulator (or) dielectric material.

→ MOS capacitor operates w.r.t "flat-band-voltage".

→ The voltage at which there is no charge on capacitor plates, and hence no electric field across SiO_2 layer is said to be "flat-band-voltage."

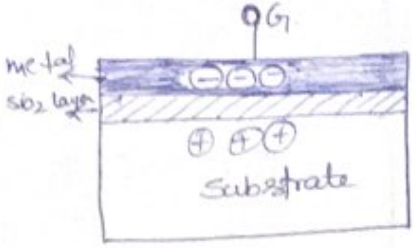
→ The capacitance of mos capacitor depends on gate voltage.

Case(i): An applied (+ve) gate voltage more than flat-band voltage ($V_{gb} > V_{fb}$). induces (+ve) charge on metal and (-ve) charge on substrate.



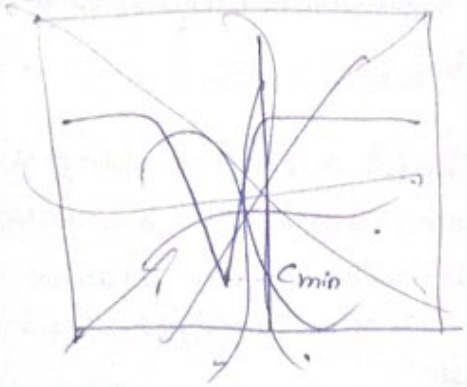
→ As negative charge accumulate at the surface, this is known as "surface accumulation"

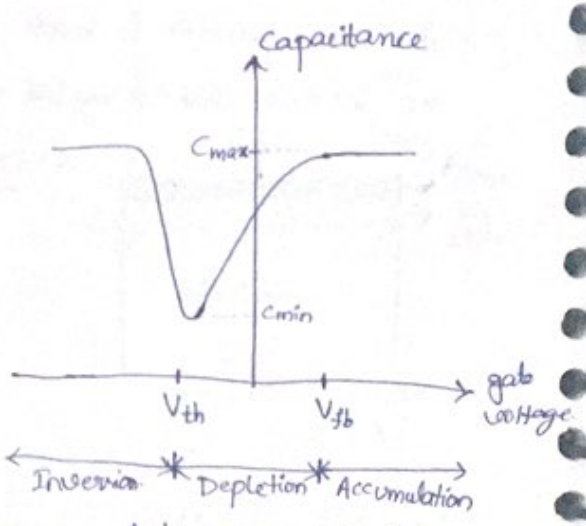
Case(2): An applied (+ve) gate voltage less than flat-band-voltage ($V_{gb} < V_{fb}$) induces negative charge on metal and positive charge on substrate.



→ (+ve) charge on substrate is due to the movement of negative electrons away from substrate surface, this is known as "surface depletion".

→ capacitance - voltage characteristics of MOS capacitor are shown below





→ flat-band voltage seperates accumulation region & depletion region

→ threshold voltage seperates inversion region & depletion region.

Problems :

(1) The JFET has parameters $I_{DSS} = 10\,mA$, $V_p = -5\,V$, find the value of gate to source voltage for drain current $I_D = 6.4\,mA$.

Sol: Given

$I_{DSS} = 10\,mA$, $V_p = -5\,V$, $I_D = 6.4\,mA$

$V_{GS} = ?$

WKT.

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$$

$$V_{GS} = V_P\left[1 - \sqrt{\frac{I_D}{I_{DSS}}}\right]$$

$$= -5\left[1 - \sqrt{\frac{6.4\times10^{-3}}{-5\,V}}\right]$$

$$= -5\left[1 - \sqrt{0.64}\right]$$

$$\boxed{V_{GS} = -1\,V}$$

(2) Given the constant $K = 0.4\times10^{-3}\,A/V^2$ of EMOSFET and $I_{D(ON)} = 3\,mA$ with $V_{GS(ON)} = 4\,V$, determine the threshold voltage V_T.

Sol: Given

$K = 0.4\times10^{-3}\,A/V^2$

$I_{D(ON)} = 3\,mA$

$V_{GS(ON)} = 4\,V$

WKT

$$I_D = K\left[V_{GS} - V_T\right]^2$$

$$V_{GS} - V_T = \sqrt{\frac{I_D}{K}}$$

$$V_T = V_{GS} - \sqrt{\frac{I_D}{K}}$$

$$= 4 - \sqrt{\frac{3\times10^{-3}}{0.4\times10^{-3}}}$$

$$\boxed{V_T = 1.261\,V}$$

EDC ASSIGNMENT - 4

SAQ:

① How FET acts as voltage variable resistor?

② What is pinch-off voltage for a JFET?

③ Draw the symbol of P-channel JFET & NPN BJT

④ Draw the characteristics of n-channel JFET & show the pinch off region on curve.

⑤ Why we call FET as voltage controlled device?

LAQ:

⑥ Explain in detail Construction & principle of operation of JFET

⑦ Explain the working of N-channel E-MOSFET

⑧ Explain V-I characteristics of JFET.

⑨ Explain drain characteristics of depletion MOSFET

⑩ Compare BJT & FET.

⑪ A FET follows relation $I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$. What is the value of I_D for $V_{GS} = -1.5V$ if I_{DSS} and V_P are given as 8.4mA & $-3V$.

⑫ Explain in detail about surface accumulation & surface depletion w.r.t MOSFET.